WHAT IS CLAIMED IS:

1. An apparatus for converting a cell format from a first format to a second format, the cell including a plurality of data bytes, the circuitry comprising:

memory;

write circuitry which is operative to receive a plurality of signals and stores the plurality of data bytes of the cell in the memory in accordance with the first format; and

read circuitry which is operative to receive a second plurality of signals and retrieve associated bytes of the stored plurality of the data bytes of the cell from the memory in accordance with the second format; wherein

the first plurality of signals do not include any of the second plurality of signals; and wherein

the second plurality of signals do not include any of the first plurality of signals.

2. The apparatus of Claim 1 wherein each of the write circuitry and the read circuitry is a state machine.

3. The apparatus of Claim 2 wherein the state machines of the write circuitry and the read circuitry provide identical state transitions.

4. The apparatus of Claim 3 wherein the states of each of the write and the read state machines are Gray encoded.

5. The apparatus of Claim 4 wherein each successive n bytes of the cell is stored in a different address location of the memory, wherein n is an integer varying between 1 and 32.

6. The apparatus of Claim 5 wherein n is 4.

7. The apparatus of Claim 6 wherein the write state machine is further operative to receive logic signals defining lengths of prepend, postpend and HEC fields of the first format of the cell.

8. The apparatus of Claim 7 wherein the read state machine is further operative to receive logic signals defining lengths of prepend, postpend and HEC fields of the second format of the cell.

9. The apparatus of Claim 8 wherein the lengths of prepend, postpend and HEC fields of the first format of the cell define the sequence of state transitions of the write state machine.

10. The apparatus of Claim 9 wherein the lengths of prepend, postpend and HEC fields of the second format of the cell define the sequence of state transitions of the read state machine.

11. The apparatus of Claim 10 wherein the write state machine and the read state machine transition through the same sequence of states if the lengths of prepend, postpend and HEC fields of the first and second format of the cell are the same.

12. The apparatus of Claim 11 wherein the sum of the lengths of the prepend and postpend fields in each of the first and second cell formats is up to 2 words and the length of the HEC field in each of the first and second cell formats is up to 1 word.

13. The apparatus of Claim 12 wherein each of the write state machine and read state machine has 12 different state transition sequences.

14. The apparatus of Claim 13 wherein in each state the write state machine generates an output signal having a binary value equal to the Gray encoded binary value of that state, wherein the output signal determines the address in the memory to which an associated 4 bytes of the cell are stored.

15. The apparatus of Claim 14 wherein in each state the read state machine generates an output signal having a binary value equal to the Gray encoded binary value of that state, wherein the output signal determines the address in the memory from which an associated 4 bytes of the cell are retrieved.

16. The apparatus of Claim 15 wherein the memory is selected from a group consisting of a static random access memory, a dynamic random access memory, a non-volatile memory and a register file.

17. The apparatus of Claim 16 wherein the cell is an ATM cell.

18. A method for converting a cell having a plurality of data bytes from a first format to a second format, the cell including a plurality of data bytes, the method comprising:

applying a plurality of signals to write circuitry to store the plurality of data bytes of the cell in a memory in accordance with the first format; and thereafter

applying a second plurality of signals to read circuitry to retrieve associated bytes of the stored plurality of data bytes of the cell from the memory in accordance with the second format; wherein

said first plurality of signals do not include any of said second plurality of signals; and wherein

said second plurality of signals do not include any of said first plurality of signals.

19. The method of Claim 18 wherein the write circuitry includes a write state machine and wherein the read circuitry includes a read state machine.

20. The method of Claim 19 wherein the write and read state machines have identical state transitions.

21. The method of Claim 20 further comprising:

Gray-encoding the states of each of the write and the read state machines.

22. The method of Claim 21 further comprising:

storing each successive n bytes of the cell in a different address location of the memory, wherein n is an integer varying between 1 and 32.

23. The method of Claim 22 wherein n is equal to 4.

24. The method of Claim 23 wherein the first plurality of signals define lengths of prepend, postpend and HEC fields of the first format of the cell.

25. The method of Claim 24 wherein the second plurality of signals define lengths of prepend, postpend and HEC fields of the second format of the cell.

26. The method of Claim 25 wherein the first plurality of signals define the sequence of state transitions of the write state machine.

27. The method of Claim 26 wherein the second plurality of signals define the sequence of state transitions of the read state machine.

28. The method of Claim 27 wherein the write and read state machines transition through the same sequence of states if the lengths of prepend, postpend and HEC fields of the first and second format of the cell are the same.

29. The method of Claim 28 wherein the sum of the lengths of prepend and postpend fields in each of the first and second cell formats is up to 2 words and the length of HEC field in each of the first and second cell formats is up to 1 word.

30. The method of Claim 29 wherein each of write and read state machines has 12 different state transition sequences.

31. The method of Claim 30 wherein in each state the write state machine generates an output signal having a binary value equal to the Gray encoded binary value of that state, wherein the output signal determines the address in the memory to which an associated 4 bytes of the cell are stored.

32. The method of Claim 31 wherein in each state the read state machine generates an output signal having a binary value equal to the Gray encoded binary value of that state, wherein the output signal determines the address in the memory from which an associated 4 bytes of the cell are retrieved.

33. The method of Claim 32 wherein the memory is selected from a group consisting of a static random access memory, a dynamic random access memory, a non-volatile memory and a register file.

34. The method of Claim 33 wherein the cell includes 53 bytes.

35. The method of Claim 34 wherein the cell is an ATM cell.